UNIT – INTRODUCTION

The Maintenance Manual (MM) is used for intelligent maintenance of the БЗУНП355Г protection-and-control unit and keeping it always ready for use.

The MM contains description of the design and principle of operation, technical data, servicing and maintenance instructions, as well as information essential for transportation and storage of the units.

The scope and intervals of maintenance operations to be performed on the unit shall be found in the Maintenance Schedule for the unit.

Given below are symbols and abbreviations used in the text:

БС	– mains;
Вг	– generator excitation;
Вкн	– GENERATOR ON (ГЕНЕРАТОР ВКЛЮЧЕН switch (load contactor switch);
Btest	– TEST (КОНТРОЛЬ) switch;
Возб	– unwanted oscillations;
Впр	– parallel operation switch;
ВСК	– built-in self-test;
ДU↓ (ДU↑ – U↓ (U↑))	– protection inhibition;
кв	– auxiliary contact;
К.З.	– short;
Кн	– load contactor;
Кпр	– parallel operation contactor;
Нпр	– parallel operation fault;
Н	– fault or response to a test stimulus (С.К.);
0	– zeroing;
ПОС	– anti-icing system;
ПР	– parallel operation;
С.К.	– test stimulus;
∆J	– current imbalance;
Uпдв	– pilot exciter voltage;
Uшг	– voltage across generator buses;
∆U	– voltage unbalance;
U↑	– elevated voltage;
U↓	– decreased voltage;

f↓	– lowered frequency;
f.g.	– functional group;
Y = X1+X2 +...	– logical addition function taking on a value of logic "1" in case even one of variables Xi takes up a value of logic "1";
Y = X1.X2	– logical multiplication function taking on a value of logic "1" in case all variables Xi take up a value of logic "1";
$Y = \overline{X}$	– inversion function taking up values opposite to variable X values;
$Y = X\tau$	– delay function taking up a value equal to X following time τ after measuring a value of variable X.

БЗУНП355Г
MAINTENANCE MANUAL

UNIT – DESCRIPTION AND OPERATION

1. GENERAL

1.1. PURPOSE

The БЗУНП355Г protection-and-control unit (Ref. Fig. 1) is used in the three-phase unstable frequency AC generating systems in which generators operate separately or in parallel after being preliminarily phased and installed on one drive.

Protection-and-Control Unit БЗУНП355Г
Figure 1

1.2. MAIN TECHNICAL DATA

1.2.1. Supply voltage:

– DC – 24.0 to 29.4 V

– three-phase AC of 690 to 840 Hz (phased) – 13.0 to 30.0 V (at R_{ph} = 11 ohms).

Quality of the unit supply voltage shall conform to 19705-89).

NOTE: The voltage varies with frequency, the lower limit complies with the least frequency and the upper, with the maximum one.

1.2.2. The unit drain current at the maximum load:

– DC – 4.0 A, maximum,

– three-phase AC of 690 to 840 Hz – 2.4 A, maximum.

1.2.3. The unit ensures:

(a) supply of a signal to trigger the generator excitation when the following conditions are satisfied:

– the generator switch is in the TEST (КОНТРОЛЬ) or GENERATOR ON (ГЕНЕРАТОР ВКЛЮЧЕН) position;

– generator has reached a rotational speed matching a frequency of 370 to 380 Hz.

(b) supply of a signal to trigger the load contactor (Кн) with generator switch (Вкн) in the GENERATOR ON (ГЕНЕРАТОР ВКЛЮЧЕН) position, GENERATOR EXCITATION signal (Вг) supplied, an effective value of generator phased voltage (an average of three phases) of 108 to 114 V reached.

(c) supply of a signal which goes to parallel operation contactor (Кпр) and anti-icing system supply contactor (ПОС) when the following conditions are satisfied:

– - contactor triggering command Кн is produced;

– PARALLEL OPERATION (ПАРАЛЛЕЛЬНАЯ РАБОТА) switch is closed;

– current imbalance H∆J signal from either of paralleled channel is absent from the protection;

– voltage drop signal or line voltage unbalance signal furnished at a time at delay of 2 s is absent;

(d) irreversible disabling of excitation of the generator and contactor Кн and taking off a signal from contactors Кпр and ПОС:

– upon opening of the generator switch;

- at a short in the generator or generator feeder in an area in which a differential protection is provided at an AC voltage higher than (1.6 to 2.0) V applied to the protection input via the diode;
- at an effective phased (average of three phases) generator voltage lower than (104 ± 3) V at a time delay of (6.0 ±0.9) s; contactors Кпр and ПОС are opened some (2.0 ±0.3) s later if the INHIBITION signal is absent;
- at an effective phased (average of three phases) generator voltage higher than (126 ±3) V at a time delay of (0.4 ±0.1) s;
- during individual operation of the generator in the presence of line voltage unbalance exceeding 20 to 40 V at a time delay of (4.0 ±0.6) s.

(e) reversible disabling of excitation of the generator and contactor Кн, picking off a signal from contactors Кпр and ПОС with the generator frequency lowering down to 349 to 361 Hz without a time delay;

(f) Disabling (in case of parallel operation) of disabling of excitation and contactor Кн:

- upon a drop of phased (average of three phases) generator voltage decrease to less than 104 ±3 V if a reactive current of the given generator exceeds an average value of reactive current of parallel-operating generators by a value causing a current higher than 10 mA at the discriminator input;
- upon a rise of phased (average of three phases) generator voltage decrease to less than 104 ±3 V if a reactive current of the given generator exceeds an average value of reactive current of parallel-operating generators by a value causing a current higher than 10 mA at the discriminator input;

(g) irreversible picking off signals Кпр and ПОС at a time delay of (2.0 ±0.3) s at a difference of total current of the given generator and an average total current of parallel-operating generators causing a current higher than 65 to 75 mA at the protection input;

(h) irreversible picking off signals from contactors Кпр and ПОС at a time delay of (2.0 ±0.3) s at a generator voltage drop (U↓) or at line voltage unbalance across the generator buses (ΔU) if the INHIBITION signal is absent;

(i) removal of disabling of the protection which has operated and a repeated triggering of the generator upon opening and a repeated closing of the generator switch;

(j) removal of disabling of the protection which has operated in case of current imbalance, U↓ or ΔU at a time delay of 2 s and a repeated triggering of the generator into parallel operation along with power supply to the ПОС upon opening and a repeated closing of PARALLEL OPERATION (ПАРАЛЛЕЛЬНАЯ РАБОТА) switch (Впр);

(k) automatic check of all protections except for the protection against total current imbalance, upon setting the generator switch to the TEST (КОНТРОЛЬ) position;

(l) pilot exciter AC voltage rectifying and supply of rectified voltage to the switching equipment of generation channel;

(m) supply of fault signals upon operation of the following protections:

$H_{кз}$ – a short in the operating area of the generator and its feeder differential protection;

HF↓ – slow down of generator rotational speed;

H∆U – voltage unbalance across the generator buses;

HU↓ – drop of generator voltage;

HU↑ – rise of generator voltage (in case the protection disconnects excitation when the voltage grows two signals HU↑ and HU↓ can appear at one and the same time).

1.2.4. The frequency protection operates from the pilot exciter whose voltage frequency is proportional to the drive rotational speed and is equal to 800 Hz at a generator voltage frequency of 400 Hz.

1.2.5. The voltage of radiointerference produced by the unit does not exceed the values specified in Table 1.

Table 1

Frequency, MHz	Voltage of radiointerference, dB to 1 μV	
	AC circuit	DC circuit
From 0.15 to 0.50	548	50
Over 0.50 to 2.50	50	44
Over 2.50 to 300.00	44	36

1.2.6. Operating mode – continuous.

1.2.7. Mass – 3.3 kg, maximum.

1.3. OPERATING CONDITIONS

1.3.1. The unit ensures safe operation under the following conditions:

(a) at a relative humidity of up to 98 % and a temperature of up to +40 °C;

(b) at an ambient temperature of:

– from +60 to –60 °C, operating,

– from +80 to –60 °C, maximum;

(c) at a thermal cycling from +80 to –60 °C;

(d) at an atmospheric pressure of up to 77 mm Hg;

(e) when exposed to hoarfrost and dew;

(f) when attacked by fungus;

(g) when exposed to a sea fog;

(h) when affected by special factors.

1.3.2. When subject to a detrimental effect

(a) the unit shows vibration resistance and vibration strength in the frequency range from 5 to 300 Hz at g-loads of up 5 g and amplitude of up to 1 mm;

(b) the unit shows resistance to impacts and impact strength at g-loads of up to 12 g at pulse duration of 5 to 15 ms;

(c) the unit is resistant to linear accelerations of up to 10 g.

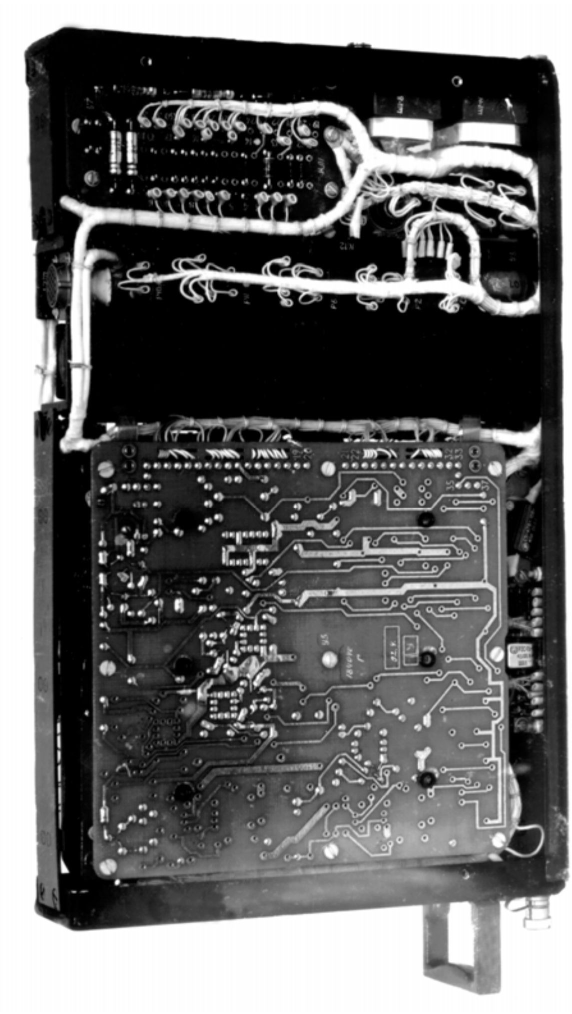
2. DESCRIPTION

2.1. Design

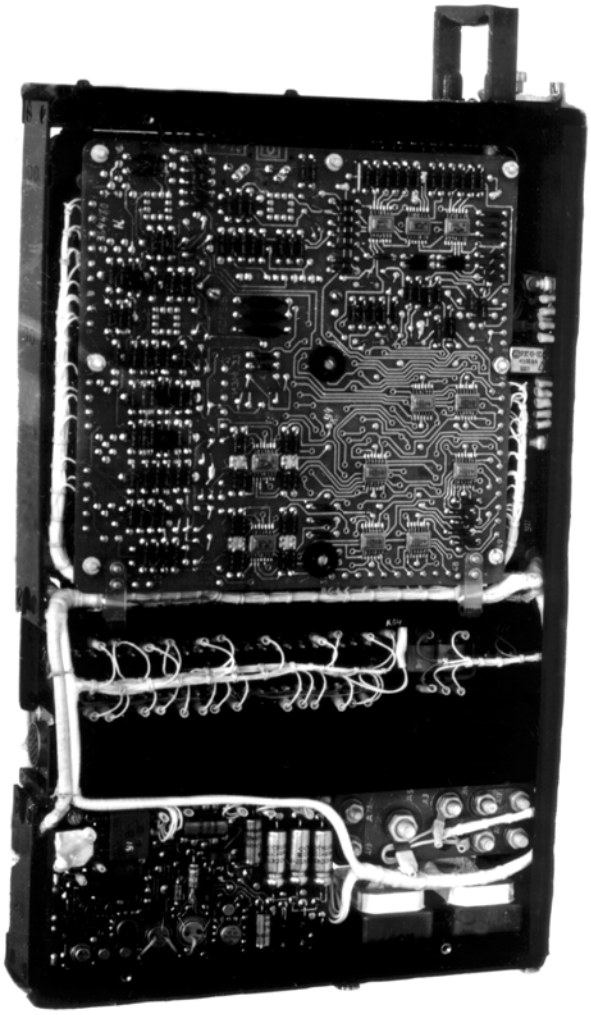
The БЗУНП355Г unit (Ref. Figs 2, 3) is a set of electrically connected functional units and elements. Secured to the face panel of the unit is a handle to pull out the unit, a stop to attach the unit with a shockmount union nut and an earthing terminal.

Found on the unit rear panel is a plug of connector Ш1 for connection with the shockmount and an expanded steel bushing for fixing and mechanical attachment of the unit to the shockmount. The position of index bushings of plug Ш1 conforms to code 07 of 26765.16-87.

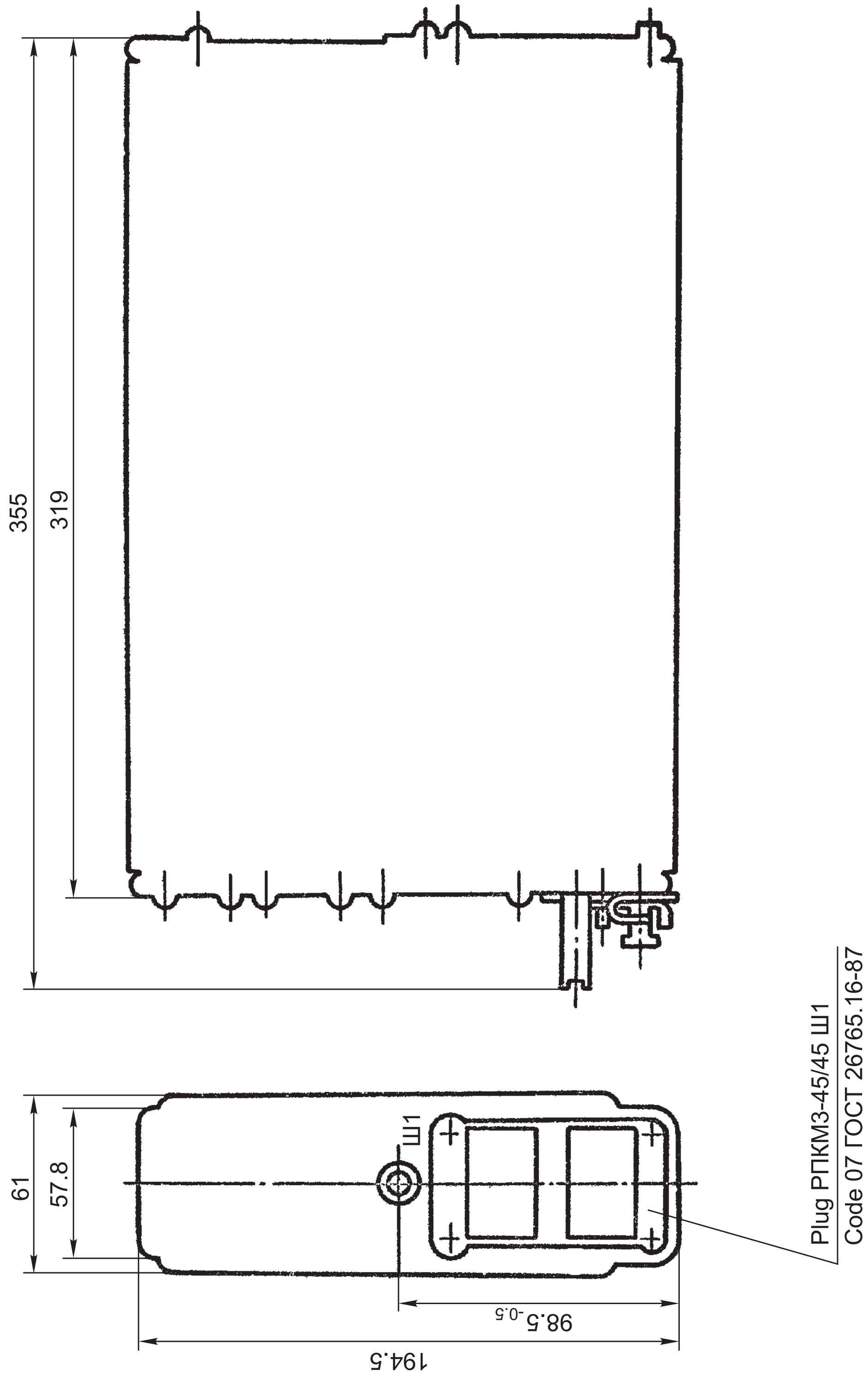
The unit is closed with two covers, which are secured with the screws, and sealed.



БЗУНП355Г Unit without Cover
(Right-Side View)
Figure 2



БЗУНП355Г Unit without Cover
(Left-Side View)
Figure 3



Overall and Mounting Dimensions of БЗУНП355Г Unit

Figure 4

3. OPERATION

3.1. General

To follow the description of operation of the БЗУНП355Г unit, consult the functional (Ref. Fig. 5) and schematic (Ref. Fig. 6) diagrams.

The БЗУНП355Г unit comprises the following functional units:

– БСГБ1Б individual operation unit (У4);

– БСГП1Е parallel operation unit (У5);

– БСЛ800ГБ frequency protection unit (У2);

– БУС9Б amplifier unit (У3);

– ПСБ2 regulator board (У1).

Found separately are electromagnetic relays with diode windings used to shunt the relays, isolation transformers, power diodes and resistors used to limit input signal current, as well as a built-in test circuit and noise filter.

Found in unit У4 are:

(a) sensors of:

- undervoltage U↓;
- overvoltage U↑;
- short,
- voltage unbalance ∆U;
- zeroing circuit;

(b) time relays set to:

- 6 s, for U↓ allowing resetting to
- 0.4 s, for U↑,
- 4 s, for ∆U;

(c) signal logic:

Вг – generator excitation;

Кн – command which goes to the load contactor;

HU↓ – undervoltage fault;

HU↑ – overvoltage fault;

H∆U – line voltage unbalance fault;

$H_{к.з.}$ – short in the differential protection operating area;

HΣ – fault of any of the protections (total fault).

Besides, found in unit У4 are elements essential for shaping a signal, which goes to the tie contactor. These are found in the БЗУНП355Г unit.

Designed into unit У3 are amplifiers for all output signals of unit У4 and Кпр of unit У5.

Unit У5 includes:

– discriminator supplying the logic protection in unit У4 with inhibitions ДU↓ and ДU↑ versus undervoltage and overvoltage, accordingly;
– meter (sensor) of current imbalance (ΔJ) of parallel-operating generators;
– protection logic versus current imbalance, undervoltage and ΔU at a time delay of 2 s;
– signal logic to contactors Кпр and ПОС;
– signal amplifier ПОС.

Unit У2 incorporates:

– lower frequency f↓ sensor;
– protection long Hf↓;
– power amplifier for monitoring signal Hf↓.

Regulator board У1 provides power of 12.6 and 5 V of the БЗУНП355Г unit.

3.2. PREPARATION OF CIRCUIT FOR OPERATION (ZEROING)

Prior to shaping a command, make sure that the level of supply voltage of logic elements falls within tolerance, all the flip-flops and memory circuits are set to the initial position. Setting the flip-flops to the initial position (ZEROING) is performed by applying logic "0" to one of the input of each flip-flop.

The zeroing circuit (Ref. Fig. 5) produces zeroing (logic "0") right after it receives +27 V through the generator switch and it lasts till the power source becomes operationally ready in channel 5 V.

In case zeroing is present, the f↓ sensor produces a signal indicating that the frequency is abnormal. This hinders applying excitation (Вг). The absence of the Вг signal inhibits operation of all the protections.

To return the circuit to the initial state at the end of self-test mode, zeroing is achieved by applying +27 V to contact 12 of unit У2 (f↓ inhibit operation) via resistor R23 (Ref. Fig. 6) and to contact 64 of unit У4. The level of voltage of 5 V and the position of the generator switch are of no importance.

3.3. SHAPING SIGNAL ВГ

To excite the generator, apply power to the exciter inductor which is energized via the voltage regulation unit (БРН) with the pilot exciter rectified voltage.

The excitation circuit is interrupted in the БРН by the contacts of a relay controlled from the БЗУНП355Г unit.

A command to apply excitation БРН is shaped in unit У4 wherefrom (terminal 46) it is fed to terminal 5 of unit У3. Then amplified signal Вг goes from terminal 7of unit У3 to trip relays P3 and P13. Signal Вг comes out of unit У4 via pin 24B of the connector plug and goes to unit У4 via resistor R5 and terminal 25. The shaping logic of signal Вг is shown in the functional diagram (Ref. Fig. 5) with the help of f. g. 9 and is expressed by the equation given below:

$$\text{Вг} = (\text{Вкн}+\text{Вконтр}) \cdot \overline{0 + f\downarrow} \cdot \overline{\text{Н}\Sigma}$$

Signal Вг is shaped when the following conditions are satisfied:

- the generator switch is moved to the GENERATOR ON (ГЕНЕРАТОР ВКЛЮЧЕН) or TEST (КОНТРОЛЬ) position (see power supply of relay P3, Fig. 5);
- zeroing is cancelled;
- the generator rotational speed is normal, that is the f↓ is absent;
- there is no trouble at all.

Signal 0+f↓ comes to f. g. 9 from f.g. 30. So, signal f↓ indicating that the frequency is abnormal is supplied at an applied zeroing as well. Thus application of Вг without checking the frequency is prevented owing to insufficient level of integrated circuit power.

3.4. CONTROL OF CONTACTOR КН

Contactor Кн receives a triggering command from the closing contacts of relay P2 via pin 27B of the plug connector of the БЗУНП355Г unit. Relay P2 is energized by signal Кн shaped in units У4 and У3 (f. g. 5, 8 and 28 – Ref. Fig. 5). The shaping logic of signal Кн is described by a logical equation given below:

$$\text{Кн} = \text{Вкн.Вг}\,((\overline{U\downarrow} + \overline{0.\text{Кн}}) \cdot \overline{0\text{БН}} \cdot \overline{3\text{Кн}})$$

Signal Вн indicating that the switch is in the GENERATOR ON position goes via pin 43B and resistor R7 (Ref. Fig. 6) to terminal 36 of unit У4.

Signal Вг shaped in compliance with equation (1) goes to terminal 25 of unit У4 via resistor R5 from the contacts of relay P3.

A parenthesized form – Ref. equation (2), means that signal Кн is produced if the generator voltage is not as low as $\overline{U\downarrow}$. This signal is locked out by signal Кн fed via resistor R3 to unit У4 to terminal 35 from the contacts of relay P2. This pickup takes place only on the removal of zeroing ($\bar{0}$), that is, when a false operation of integrated circuits is impossible owing to a low level of power.

The closing contacts of relay P2 trip the coil of relay P10 powered with +27 V via "Indication power" pin 3B. Signals Кн as +27 V are taken out to pins 28B, 23H, 45H.

3.5. CHANNEL EMERGENCY DISCONNECTION

An emergency disconnection of the channel is essential for avoiding a low-quality power supply to the using equipment.

Disconnection of the channel implies taking off signals Вг and Кн which leads to disconnection of contactor Кпр.

Power quality control is performed with the help of the БЗУНП355Г unit sensors. As a sensor of a respective protection operates, the logic receives a signal which activates a time delay (Table 2) on expiring of which a channel emergency disconnection takes place.

Table 2

Time delay for different types of protection

Protection	Time delay, s	Signal
A short producing UDC ≥ 2.0 V across the protection input in an area to which a differential protection is connected	W/o time delay	К.З.
Generator frequency lower than 349 to 361 Hz	W/o time delay	f↓
Line voltage unbalance > 20 to 40 V	4.0 ±0.6	ΔU
At the generator voltage lower than (104 ±3) V after fir voltage rise in excess of (111 ±3) V	6.0 ±0.9	U↓
At the generator voltage higher than (126 ±3) V	0.4 ±0.1	U↑

After operation of any of the protections except for the f↓ protection, total fault signal HΣ which has disconnected the channel is stored. To disconnect the channel for a second time, cancel the disabling by opening the generator switch.

On opening the generator switch, all the memory circuits shall be zeroed (set to the initial state).

The shaping logic of fault signals is described by equations (3 to 8) below:

$$Нк.з. = (Вкн+Вконтр) \cdot (Вг \cdot К.З.+Нк.з. \cdot \bar{0} \quad (3)$$

$$НU\uparrow = (Вкн+Вконтр) \cdot [(Вг \cdot U\uparrow \cdot \overline{DU\uparrow \cdot КВКпр})^{0.4\,c} + НU\uparrow \cdot \bar{0}] \quad (4)$$

$$НU\downarrow = (Вкн+Вконтр) \cdot [(Вг \cdot U\downarrow \cdot \overline{DU\downarrow \cdot КВКпр})^{6\,c} + НU\downarrow \cdot \bar{0}] \quad (5)$$

$$Н\Delta U\downarrow = (Вкн+Вконтр) \cdot [(\Delta U \cdot \overline{КВКпр})^{4\,c} + Н\Delta U \cdot \bar{0}] \quad (6)$$

$$Нf\downarrow = (Вкн+Вконтр) \cdot (f\downarrow+0) \cdot Зf \quad (7)$$

$$Н\Sigma = (Вкн+Вконтр) \cdot [(Вг \cdot К.З.+(Вг \cdot U\uparrow \cdot \overline{DU\uparrow \cdot КВКпр})^{0.4\,c} + (Вг \cdot U\downarrow \cdot \overline{DU\downarrow \cdot КВКпр})^{6\,c} + [(\Delta U \cdot \overline{КВКпр})^{4\,c} + Н\Sigma \cdot \bar{0} \cdot \overline{ЗН\Sigma}] \quad (8)$$

Channel disconnection is performed in compliance with equation (1) when signal НΣ appears (Ref. equation (8)). Disconnection irreversibility is ensured by the last addend in equation (8). The memory of each fault of the indication is provided by the presence of the second addend in equations (3 thru 6).

Operation of the memory is inhibited upon application of zeroing. For this purpose second addends in equations (3 thru 6) take up cofactor $\bar{0}$.

To improve the noise immunity of the protections, the augends of equations (3 thru 5) take up cofactor Вг. The existence of this cofactor also prevents the operation of protection versus U↓ upon disconnection of the channel.

Logic equations (3 thru 8) are illustrated by a functional diagram given in Fig. 5.

Signal К.З. is shaped by the sensor after measuring a signal coming via pins 14B and 35B to the БЗУНП355Г unit from the current transformer unit (БТТ). A signal from the БТТ unit is proportional to the difference in secondary currents of the current transformers of the differential protection.

Signal К.З. is applied to the input of f.g. 4 (Ref. Fig. 5) shaping signal $Н_{К.З.}$ in compliance with equation (3).

Signals НU↓ and НU↑ are shaped with the help of the signals which go from the discriminator, namely: ДU↓ and ДU↑ inhibiting operation of the protections versus U↓ or U↑ depending on a ratio of current reactive components of parallel-operating generators.

In f.g. 1, 2 the inhibiting signals from the discriminator are multiplied with signal квКпр which inhibits operation of inhibiting signals during isolated operation of the generators.

Signals U↓ and U↑ come to the inputs of f.g. 6, 7 from the sensors measuring the level of generator voltage. The generator voltage is fed via pins 7B, 10B, 13B to the БЗУНП355Г unit and transformer Tp3from the adjustment point – input terminals Кн.

F.g. 6, 7, 10 thru 12 are used to shape signals HU↑ and HU↓ in compliance with equations (4) and (5).

For shaping signal HΔU, a voltage is supplied via pins 20B, 23B, 26B from the generator buses and transformer Tp2 to the БЗУНП355Г unit.

Signal ΔU goes from the voltage unbalance meter to the input of f.g. 3 (Ref. Fig. 5). Signal кв$\overline{Кпр}$ inhibiting operation of the protection versus ΔU during parallel operation has the same address.

From the output of f.g. 3 the signal goes to the input of time relay at the output of which signal HΔU is shaped in compliance with equation (6).

The pilot exciter line voltage is fed via pins 4B and 42B and transformer Tp1 to the input of unit У2 to terminals 8 and 7. Signal Hf↓ is applied from the output of f.g. 30 without a time delay in compliance with equation (7). All the four fault signals are summed up at the f.g. 13 at the output of which signal HΣ is obtained in compliance with equation (8).

To amplify the signals shaped in unit У4), use is made of unit У3. Signals HU↑, HU↓, $H_{К.З.}$, HΔU and HΣ coming from the amplifier energize relays P9, P8, P4, P5 and P7, accordingly.

The fault signals go from the relay contacts to the built-in test circuit (BCK) as well as to unit У3 to be used for memory organization (Ref. the second addends of equations (3 thru 6 and 8).

For the built-in test circuit to register the operation of the frequency protection, signal Hf↓ is amplified with the help of an amplifier arranged in the same way as the meter and the logic of this signal in unit У2.

Fault simulation during operation of the BCK is performed by application of test stimuli (C.K.) to the sensors. On applying a stimulus, the sensor circuit is re-arranged so that at normal voltage (or frequency) parameters the sensor produces a signal indicating that the parameter is abnormal.

Signals essential for unit regulation are taken off the sensors to test connector Ш2 of the БЗУНП355Г unit.

3.6. PROTECTION SERVICEABILITY BUILT-IN TEST

The built-in test (BCK) is run each time the generator switch is moved from the GENERATOR ON to TEST position within 5 s. After the test a signal is fed via pin 4H to the CHANNEL OK (КАНАЛ ИСПРАВЕН) lamp.

The test is run by simulating faults in the generating system with the help of C.K. applied to the sensors. When all the protections operate, the C.K. are taken off. The memory circuits are set to the initial state by applying zeroing.

To avoid taking off signal Bг by the frequency protection which is likely to occur during the test, the INHIBITION f↓ signal is fed via diode Д45 from the closing contacts of relay P16 along with a stimulus applied to terminal 11 of unit У2 since there is internal connection between terminal 2 and terminal 11 of unit У2. Signal INHIBITION f↓ is applied much in the same way simultaneously with application of zeroing to terminal 12 of unit У2 from the closing contacts of relay P14. In the systems where the frequency protection is not required this signal is applied via pin 3H to unit У2.

The BCK operates as follows.

After closing the B_{test} switch, regulator board У1 becomes energized. As long as the regulator becomes operationally ready, zeroing is generated. On receiving zeroing the logic of signal Bг receives an abnormal frequency signal from unit У2. This condition does not allow signal Bг to appear (Ref. equation (1)).

The coil and contacts of relay P13 are energized through the B_{test}. This relay is energized much in the same way as relay P3, that is in response to signal Bг. Since signal Bг has not been produced yet, relays P16 and P17 are energized via the opening contacts of relays P13 and P20. The closing contacts of relay P17 feed power to the coils of relays P16 and P17 by signal $\overline{\Sigma Hi} = \overline{Hf\downarrow} + \overline{H_{k.з.}} + \overline{HU\downarrow} + \overline{HU\uparrow}$, that is, as long as all the faults exist.

Signal $\overline{\Sigma Hi}$ is obtained by summing up the signals coming from the opening contacts of relays P1, P4, P5, P8 and P9.

The closing contacts of relay P16 prepare the circuit for producing the C.K. to sensors ΔU and f↓. In case the regulator, zeroing circuit, logic and amplifier of signal Bг are OK, the regulator becomes operationally ready, zeroing is cancelled, signal Bг is produced, that is relay P13 trips. The C.K. is produced via the closing contacts of relays P13 and P16, diodes Д42 and Д45 to sensors ΔU and f↓. At the same time inhibited is the output of f↓ to logic Bг.

After relay P13 trips, it becomes self-latched. Along with the delivery of the said stimuli relays P15, P14 and P20 become energized and self-interlocked by signal $\Sigma Hi = Hf\downarrow + H_{К.З.} + H\Delta U + H\uparrow + H\downarrow + H\Sigma$ as long as even one fault exists. If the channel is free from active failures of quick-operating protections (C.K. or U↓) excitation is not disconnected until the ΔU protection operates. Four seconds later operation of the ΔU protection results in disconnection of excitation (relay P13 drops out). The coil of relay P18 is energized via the opening contacts of relay P13. The contacts of relay P18 energize relay P19 feeding the stimuli via diodes Д43, Д41 and Д40 to sensors К.З., U↑, U↓. This very circuit supplies a parallel operation signal enabling operation of the discriminator, as well as a total fault inhibition. The total fault inhibition results in application of excitation (relay P13). The coils of relays P16 thru P19 are kept energized until all the protections operate. Signals HU↑ and HU↓ appear at a time delay of 0.4 ±0.1 s. After all the faulty occur, the relays drop out which results in taking off the stimuli, as well as inhibition HΣ but at a delay ensured by capacitor C5. The opening contacts of relay P16 and closing contacts of relay P14 supply zeroing to the fault memory. After the relays of all faults drop out, the coils of relays P14, P15, P20 become de-energized.

As this occurs, zeroing is cancelled at a delay supplied by capacitors C6, C7 to set the metering elements of protections to the initial state. The channel serviceability signal is produced via the closing contacts of relay P13 and opening contacts of relays P16, P14, pin 4H and resistors R31 thru R33 limiting the lamp starting current.

3.7. Shaping command for contactor Кпр and power application to ПОС

To switch the generator in parallel operation or to supply power to the ПОС, close the PARALLEL OPERATION (ПАРАЛЛЕЛЬНАЯ РАБОТА) switch. In this case, 27 V shall be supplied to pin 44H. In the systems where parallel operation is not provided, pin 44H receives signal Вкн to energize the ice-protection system. The logic of signals Кпр and ПОС is similar. Signal Впр comes to terminal 16 of unit У5. The next necessary criterion for signals Кпр and ПОС to appear is existence of a command across Кн. Since the command includes signal Вг, the existence of which implies a trouble-free state, disconnection of the Кпр is provided in case of channel emergency disconnection.

To energize the Кпр and supply power to the ПОС, the absence of a fault signal is necessary in addition to application of signals Впр and Кн. An equation for the Кпр ПОС is as follows:

$$\text{Кпр (ПОС)} = \text{Впр Кн } \overline{\text{Н}}\text{пр} \qquad (9)$$

A parallel operation signal shaped in f.g. 34 in compliance with equation (9) goes via terminal 22 of unit У5 to pin 5B of the БЗУНП355Г unit. When pins 5B of the БЗУНП355Г units of parallel-operating channels are connected, serial copying of parallel operation logic is performed including the Нпр protection. Signal Кпр (or Кпр1 . Кпр2 in case pins 5B of paired БЗУНП355Г units are connected), amplified in unit У3 (Ref. Fig. 5) energizes relay Р6 which controls contactor Кпр. Besides, this signal being added with the test stimulus at f.g. 36 and amplified, triggers via terminal 14 of unit У5 relay Р11. One pair of opening contacts of relay Р11 is used to unshunt resistor R29 (Ref. Fig. 6), connected into the ΔJ protection equalizing circuit, and a discriminator. Voltage taken off resistor R29 is fed via transformer Тр4 unit У5 via terminal 3, 4 to the discriminator and via terminals 1, 2, to the input of sensor ΔJ. A voltage developed across resistor R29 is proportional to the difference between the current of given generator and an average current of parallel-operating generators. Stabilizer diodes Д18, Д19 eliminate saturation of transformer Тр4 at a large input signal. A linear voltage of the generator is essential for operation of the discriminator. It is fed to unit У5 from transformer Тр3 to terminals 10 and 12.

The closing contacts of the second pair of contacts of relay Р11 are used to feed power to the anti-icing system.

Disconnection of contactors Кпр and ПОС is effected with the help of switch Впр, as well as in case of emergency channel disconnection or failure resulting in operation of protection Нпр. Signal Нпр is shaped with the help of a meter, f.g. 32, 33, 35 and a time delay in compliance with equation (10).

$$\text{Нпр} = \{\text{Впр} \cdot [\Delta I + \text{Кн} \cdot \overline{3} \cdot (U{\downarrow} + \Delta U) + \text{Нпр}]\}^{2c} \qquad (10)$$

3.8. Regulator board ПСБ2

To follow the description of operation of the ПСБ2 board, consult the schematic diagram shown in Fig. 7.

The ПСБ2 board is used to power the assemblies of the БЗУНП355Г unit with stabilized DC voltages of 12.6 V and 5 V. The primary voltage is fed to the ПСБ2 board either from the pilot exciter via a half-wave rectifier or from the mains.

A rectified voltage supplied from the pilot exciter varies in the range from 14 to 37 V while the voltage supplied from the mains, in conformity with 19705-74.

So, the ПСБ2 board shall operate in a wide range of supply voltage from 14 to 80 V.

The ПСБ2 board is a two-stage regulator: a stabilized voltage of 12.6 V (more coarse) is derived by a sampled control while a voltage of 5 V (more fine), by a linear control of an earlier stabilized voltage of 12.6 V.

A switching regulator for U_{out} = 12.6 V consists of power transistor Т7, integrator Др3, С8, С9, reference voltage source Д6, comparator circuit R18, R19, R21 thru R26, DC amplifier У1, flip-flop Т4, Т6, R10, used to control the power transistor, and damping diode Д3.

Adjustment of the output voltage in the switching regulator is performed by changing the switching frequency of transistor Т7.

A signal to switch transistor T7 is applied from the flip-flop which operates when the reference and output voltages picked off from divider R18, R19 are unequal. The voltage difference is amplified by amplifier У1) and fed to the flip-flop input.

To match the control circuit with power transistor T7, series-connected into the darlington circuit are transistors T3 and T5.

A line regulator for 5 V consists of regulating transistor T10 and amplifier У2.

Reference voltage source Д6 is common for regulators for 12.6 and 5 V. The output voltage is regulated owing to a voltage drop change across the emitter-collector arm of transistor T10. A signal characterizing a conductance level of transistor T10 goes from the output when the output voltage across resistor R26 is compared with the reference voltage. Then it is amplified in amplifier У2 connected in the differential amplifier circuit and applied to the base of transistor T9.

Provided in the ПСБ 2 board is the current overload protection circuit built around transistors T8, T1, T2 and resistors R16, R17.

3.9. Amplifier unit БУС9Б

To follow the description of operation of the БУС9Б unit, consult the schematic diagram shown in Fig. 8.

The БУС9Б unit is designed to amplify input signals which come to its inputs from unit У4 (Ref. Fig. 5).

The БУС9Б unit consists of nine amplifiers, eight of which are used in the Б3УНП355Г unit.

As to their power, the amplifiers are divided into two types: amplifiers energizing relays, type TKH, and amplifiers, energizing relays, type TKE.

The БУС9Б unit amplifies the following signals: signal Вг – in the У5, signal HΣ – in the У6, signal Кн – in the У7, signal HU↓ – in the УМ1, signal HU↑ – in the УМ2, signal HΔU – in the УМ3, signal $H_{К.З.}$ – in the УМ4 and signal Кпр – in the У3.

The amplifiers employ a three-stage circuit with a common emitter built around transistor packs. Two last transistors of the packs are series connected to ensure protection against short-time mains overvoltages.

The closing contacts of relays energized by the given amplifier apply signal +27 V to input 2 of each amplifier УМ1 thru УМ4. Thus the fault indication memory is filled in. Memory reset is effected by applying the ZEROING signal to inputs 8 of amplifiers УМ1 thru УМ4.

Capacitors C1 found in amplifiers УМ1 thru УМ4 and capacitors C3, C5 are used to protect the amplifiers against unwanted oscillations. The INHIBITION HΣ signal comes to terminal 6 of the unit. This signal is used during the self-test of the generation channel.

To avoid a false operation of the amplifiers the moment channel switch Вкн is closed, zeroing is applied to the inputs of amplifiers Кн and HΣ.

3.10. Frequency protection unit БСЛ800ГБ

To follow the description of operation of the БСЛ800ГБ unit, consult the schematic diagram shown in Fig. 9.

Applied via step-down transformer Тр1 from the pilot exciter to the unit input (terminals 7 and 8) is a DC voltage of 800 Hz.

The frequency is measured by comparing the input signal period duration with the duration of a reference signal shaped with the help of univibrator (a single-shot multivibrator).

The shaper of square pulses of a duration equal to half period of an input signal is built around transistors of matrix У1 and transistor Т1. An input signal is filtered at a filter made up of capacitors С11, С12 and С2 (Ref. Fig. 9) and choke Др1 (Ref. Fig. 6).

Built around transistors У1 is a differential amplifier (a differential couple) with resistor R3 connected into the emitter circuit. An input signal is applied to the differential couple via resistors R1 and R2. From the differential couple output the signal is applied to the base of transistor Т1. A stage with a common emitter employing transistor Т1 is an output stage of the shaper. Besides, it helps to set up a positive feedback. The existence of a positive feedback ensures an on-off operation of the shaper. From the shaper output (the collector of transistor Т1) the square pulses of an input signal frequency are applied to T flip-flop У2.

At the output of T flip-flop У2/8 and after inversion at the У4/12 pulses of a duration equal to a period of input sinusoid are obtained. So, frequency division is accomplished to ensure independence of pulse duration of a curve form and shaper operating level.

To improve noise immunity of the circuit, connected to the shaper input are limiter diodes of matrix У9 and capacitors С2, С13, С14.

Signals go from the frequency divider to the comparator circuit with a reference univibrator pulse, as well as to trigger a univibrator built around transistors of matrix У6, У7 and transistors Т3 and Т4.

A univibrator is made up of two series-connected differential stages. The first stage built around transistors Т3 and Т4 controls the differential couple consisting of transistors of pack У6-1 with resistor R17 connected into the emitter circuit.

A reference voltage of +5 V is fed to the base of transistor Т3. The transistor of matrix У7 (terminals 8, 9, 7) sets up a positive feedback in the quasi-equilibrium mode. Triggering of univibrator is performed with the help of turning on the transistor of matrix У7 (terminals 5, 6, 4) applying logic "1" to its base from the У412.

In the initial stable state the transistors of matrix У7-1 are non-conductive, the potential of the base of transistor Т3, hence, of transistor Т4 as well is equal to 5 V.

The LH plates of the capacitors in the time-setting circuit С3 thru С9 are connected via resistor R11 to a 12.6-V source while the RH ones, to the base of transistor Т4 having a potential of +5 V. So, the capacitors are charged via resistor R11 to a level of 7.6 V. A degree of conductance of transistor Т4 is such that a transistor in the second stage (У6

– terminals 11, 10, 12) becomes conductive. Logic "1" is taken off from the collector of the said transistor (the univibrator output).

At the moment of univibrator triggering, a voltage accumulated across the capacitors is applied via the transistor of matrix У7 and resistors R12, R16 rendered conductive by an input signal to the emitter-base junction of transistor T4. This renders transistor T4 non-conductive and transistor T3 conductive. After switching the respective transistors in the second stage, a blocking voltage of the capacitor is still applied to the emitter-base junction of transistor T4 via a conductive transistor of matrix У7 irrespective of the state of input transistor until all the capacitors get discharged via the circuit: conductive feedback transistor, base of transistor T3, resistor R16, resistance of the 12.6-V source and matched resistors.

As long as transistor T4 is non-conductive, logic "0" is taken off the univibrator output. The time the univibrator puts out logic "0" is a reference time. Then comparison of the input sinusoid period (signals across the T flip-flop output) with the univibrator reference signal duration is accomplished with the help of logic elements.

A diagram presented in Fig. 10 illustrates the shaping logic of signal f↓. An output У4/12 taken off from he pulse shaper after the frequency divider (T flip-flop and inverter) shall be denoted as ФИ and an inverse value taken off У2/8 – $\overline{\text{ФИ}}$.

As logic "1" appears across output ФИ, the univibrator gets triggered (over the leading edge).

A time period during which logic "0" lasts at the univibrator output (OB) is equal to a period when a decreased frequency (f↓) exists. Used in the comparator circuit is an inverse value ($\overline{\text{0B}}$) obtained at output У5/7.

If a width of the squares across the У4/12 is less than a width of the squares across the У5/7, the frequency is normal. This is registered and filled in at time moment 3 and acknowledges at moments 4 and 5. If signal ФИ is longer than reference signal ($\overline{\text{0B}}$), the presence of f↓ is registered (Ref. time moments 6, 7, 8, Fig. 10).

The input signal-reference signal duration comparator circuit is built around two Д flip-flops in integrated circuit У3. At its output the Д flip-flop has a value inverse to the value across input Д provided logic "1" exists across input C. If logic "1" exists across input C the value across the output is stored. In case zeroing (logic "0") is applied to input R of flip-flop У3-1, logic "0" is found across output У3/2. This means that the frequency is abnormal, application of excitation without checking the frequency is inhibited. Canceling of zeroing (time moment 1 in Fig. 10) does not imply a change in the output state (the lower line in Fig. 10) until the frequency is measured (time moment 3). After canceling zeroing, signal ФИ which goes from input У2/6 changes its value when logic "0" appears across the inputs of T flip-flop. The on-off characteristic of frequency sensor is ensures by the presence of a positive feedback, which facilitates tuning away of the input signal from the frequency modulation.

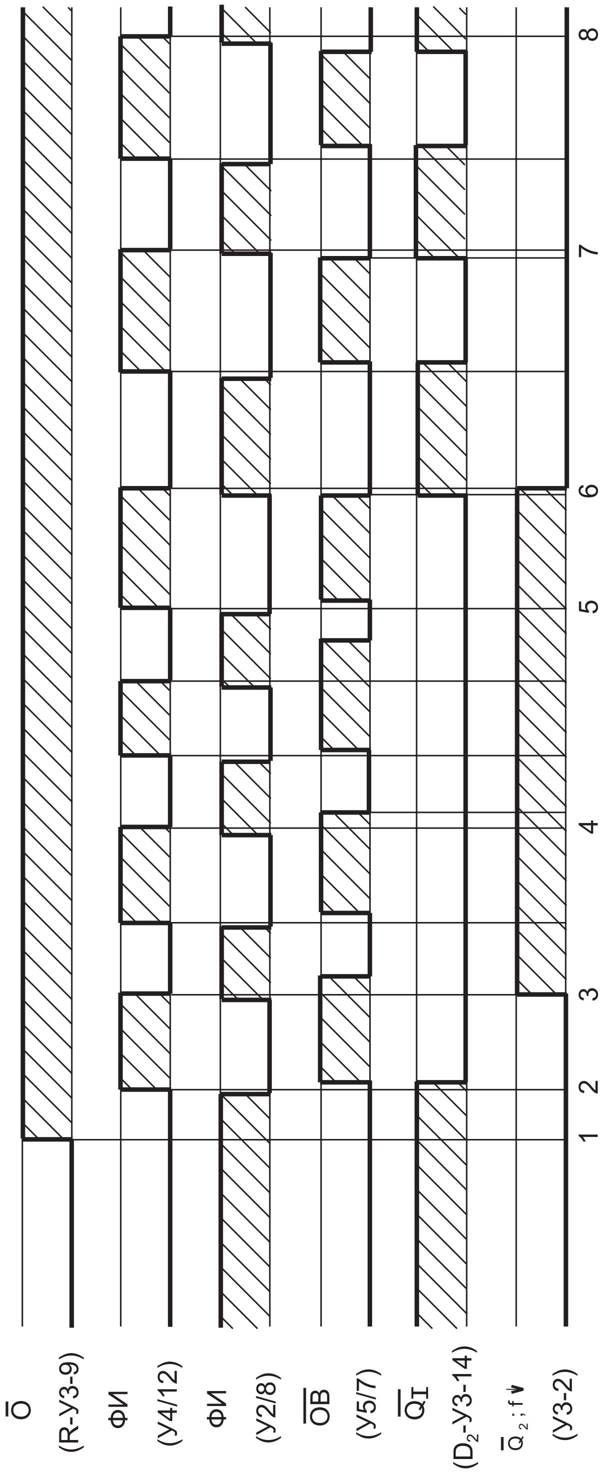


Diagram of Signal Shaping Logic
Figure 10

A feedback signal goes via inverter У4-2 to the univibrator from the comparator circuit. The switch built around the transistors of matrix У6 and У7 shunts of unshunts feedback resistor R22 series-connected with time-setting resistors.

During operation of the built-in test circuit, operation of the frequency protection versus a stimulus is achieved by parallel-connection of resistor R25. In this case, power amplifier built around the transistors of matrix У8 operates. Logic "1" is artificially backed up across the unit output (terminal 5) to keep excitation applied during the test. This is achieved by applying inhibition f↓ concurrently with the output of test stimulus (C.K. f↓ – terminal 11) and test stimulus ZEROING (terminal 12).

3.11. Isolated operation unit БСГБ1Б

To follow the description of operation of the БСГБ1Б unit, consult the schematic diagram shown in Fig. 11.

The unit incorporates the functional groups mentioned under 2.1. It performs the functions in compliance with equations (1 thru 6) and (8).

A short sensor, which is a sensitive element of a longitudinal differential protection, is built around amplifier У4 which operates as a comparator and transistors T5, T4. The divider employing resistors R28 // R25 and R27 makes up an artificial tap connected to a +5-V source. Resistors R10, R11, R16 and R17 limit the amplifier input currents. The diodes of assembly У3 limit a differential input signal. The operating level of zero-element У4 is set by a voltage drop across resistor R27 due to a current flowing from a +12.6-V source via resistor R26.

In the absence of an input signal, transistors T5, T4 are non-conductive, capacitor C7 is discharged, a signal of logic "1" is found across the sensor output.

In case of a short, a rectified half-wave circuit voltage exists across the sensor input (terminals 6 and 4 of the БСГБ1Б unit). The said voltage makes comparator У4 operate every other half period.

During operation of the comparator, output voltage У4 (output У4/5 drops below +5 V, transistor T4 becomes conductive. In this case, capacitor C7 gets charged. If a pulse is absent, the capacitor gets discharged via resistors R37 and R38. In a number of pulses a voltage across capacitor C7 reaches a value sufficient for transistor T5 to become conductive. While transistor T5 is becoming conductive, it sets up a positive feedback circuit.

The next half period when an input signal is absent transistor T5 is kept conductive owing to a discharge current of capacitor C7. So, at a short, a signal of logic "0" coming to the logic is taken off from collector T5.

To avoid a false operation of the short protection the moment a short is eliminated, capacitor C7 is connected via resistor R42 and diode Д11 to the output of the zeroing unit.

Realizing of equation (3) is accomplished as follows.

After inversion across the У20-4, a signal is fed from the sensor to input 5 of element У20-4. Applied to input 6 of the same element is signal Вг.

A simultaneous freaking of logic "1" across the both inputs causes appearing of logic "0" across the У20/7 and logic "1" across the У29/10 which means the presence of fault $Н_{К.З.}$. A signal coming from output У20/7 is an inverse value of signal $Н_{К.З.}$. It comes to fault adder У28. From the У29/10 signal $Н_{К.З.}$ is fed via terminal 38 to the БУС9Б unit which energizes relay P4 (Ref. Fig. 6).

The test of sensor and of signal $Н_{К.З.}$ logic is run by applying +27 V via the resistor to terminal 7 of the БСГБ1Б unit.

Signal H∆U is shaped in compliance with equation (6).

The said signal comes out from the БСГБ1Б unit via terminal 37 to be amplified in the БУС9Б unit while its inverse value is applied to fault adder У28. Signal H∆U appears across the output of time relay built around the transistors of matrix У24 some (4 ±0.6) s after the input transistor is turned off by logic "0" coming from element У21-2.

The time relay for signal H∆U (Ref. Fig. 12) is built around a bridge circuit whose two arms employ resistor R110 and series-connected resistors R111, R112.

Connected across the bridge made up of the said arms is a null element. The latter is a differential amplifier built around the transistors of matrix У24 and resistor R100 in the emitter circuit. Operation of the null element of time relay takes place when a voltage across the capacitive divider exceeds a voltage across the resistive divider.

A null element is a relay amplifier. It operates in the existence of a positive feedback set up by the output transistor, which shunts resistor R112 upon operation of the time delay relay. The null element controls triggering of the output transistor via transistor У22-3. A degree of elevation of the resistive divider center tap potential is limited by integration of these taps via the diode in matrix У26). This helps to protect the base-emitter junction of the differential couple transistor and to minimize the time relay reset time. A base-emitter junction series-connected with resistors R110 thru R112 is used to stabilize the relay temperature. A divider employing resistors R89, R90 and dividing diode У26 connected to it serve to set an initial voltage level across the capacitors (additional shaping) which stabilizes the rated value of electrolytic capacitor.

The capacitors are charged to a level controlled by divider R89, R90. Since a voltage across capacitor C15 is less than a voltage across the lower arm of the resistive divider, transistor of the У22-3 and the output transistor are non-conductive.

When logic "0" is applied to the input of time relay the input transistor becomes non-conductive. From this moment on, the relay starts zero time reference. Capacitor C17 gets discharged while capacitor C15 gets charged via resistors R93, R94. Operation of the time relay, that is, turning on of the output transistor takes place at the moment when the voltage across terminal 13 of matrix У24 exceeds the voltage across terminal 11. If logic "0" exists across the circuit input during a time period shorter than (4 ±0.6) s, the circuit returns to the initial state having no time for operation. Logic "0" across the У21/6 triggering the time relay appears if logic "1" concentrate across inputs 8 and 9 of element У20-1. Applied to input 9 of this element is signal ΔU from the sensor and to input 8, an inverse value of parallel operation signal квКпр to inhibit operation of the protection versus ΔU during parallel operation of the generators. In this case, contactors Кпр and ПОС become de-energized some (2 ±0.3) s later if the INHIBITION signal is absent. Applied to the sensor input from the transformer secondary windings each having a center tap are three levels proportional to the phased voltages across the generator buses. The center taps of transformer secondary windings are interconnected, a common tap being connected to terminal 15 of the unit. A secondary voltage supplied to the unit via terminals 10 and 11 is rectified in a full-wave circuit across diodes Д5, Д6 and smoothed across a L-shaped filter. In this way a DC voltage of a value proportional to one of the phased voltages is obtained across capacitor C3. In much the same way capacitors C1 and C2 are charged to levels matching the voltage of two other phases. The voltage levels across capacitors C1 thru C3 whose RH plates are connected to terminal 15 are compared one with another with the help of the diodes in matrixes У5 and У6.

In case of phased voltage unbalance exceeding the norm, a current flowing through resistors R41 and R43 causes a voltage drop across resistor R43 which lowers the potential transistor T6 base as compared with the level of +5 V below the potential of transistor T7 base. This causes turning on of transistor T6 and turning off of transistor T7 and, hence, of transistor T8 as well. Picked off from the collector of transistor T7 is signal ΔU.

In case an input voltage is absent or phased voltages are equal, transistors T8 and T7 are conductive while transistor T6 is non-conductive owing to power tilt of the amplifier which occurs due to connection of transistor T7 base with the common "minus" via resistor R48. On-off operation of the sensor is ensured by a positive feedback set up between transistors T7 and T8. When the sensor is under test, its operation is provoked by connecting transistor T6 base via resistor R41 and the contacts of relay P1 to the coil of which the C.K. is applied to the common wire.

Signals HU↓ and HU↑ shaped in compliance with equations (5) and (4) come out of the БСГБ1Б unit via terminals 39 and 40.

An inverse value of these signals is applied to input 8 of fault adder У28 at a time delay common for these protections. The time relay for signals HU↓ and HU↑ is built around the transistors of matrixes У23 and У22 in a circuit similar to the time relay for signal HΔU and is rated for a delay of (6 ±0.9) s at U↓ When triggered from signal U↑ it is set to a delay of (0.4 ±0.1) s. Re-setting is accomplished by application of signal U↑ to terminal 8 of matrix У23. In this case a switch built around transistor У22-1 and the transistor of matrix У23 connects resistors R95 and R96 in parallel to resistors R97 and R98. Triggering of a time delay is accomplished by logic "0" freaking across output У21/12 if signal Br is applied to input 14 of this integrated circuit and logic "1" exists across input 13 indicates that signal U↓ or U↑ exists. However signals U↓ and U↑ may be inhibited by signals coming from discriminator ДU↓ and ДU↑. The inhibit operations run in integrated circuits У19-1 and У17-3. The discriminator inhibitions ensuring selectivity of emergency disconnection during parallel operation are effective only in the presence of a signal from an auxiliary contact of the parallel operation contactor. This signal comes to inputs 6 and 3 of integrated circuit У17.

Elevated or lower voltage sensors of the generator have a one-type circuit. The latter incorporates an ic amplifier and two switching transistors to which a positive feedback is applied.

The generator voltage rectified by the diode bridge is filtered by L-shaped filters and supplied to inputs 9 of amplifiers У7 and У11. Applied via resistors R54 and R65 to inputs 10 are a reference signal of +5 V and a positive feedback signal from the collectors of transistors T10 and T12 via resistors R56 and R67. If a voltage is normal, it is higher than a reference voltage across input У7/9, the output voltage of the amplifier is below the +5-V level which results in turning on of transistors T9 and T10.

Logic "0" obtained in this way across collector T10 testifies to the absence of a reduced voltage. AT a normal voltage the potential across input У11/9 is higher than across У11/10. This leads to output of logic "1" from collector T12 which means that there is no elevated voltage. As the voltage decreases, logic "1" appears across the output of sensor U↓ and as the voltage becomes high, logic "0" across the output (collector T12) of sensor U↑. Diodes Д22 thru Д25 limit a differential signal. Diodes Д18, Д19 fed via resistor R49 serve to control temperature of the rectifier diode.

Capacitors C9, C11 are used as HF noise filters in the amplifier supply circuit. Adjustment of the operating level for the sensors is performed with the help of variable resistors R50 and R6. The test stimuli are fed to the coils of relays P2 and P3. The relay contacts are connected to one of the arms of the input signal divider, a resistor is connected to re-adjust the divider so as to make the sensor operate at a normal generator voltage. A switch employing transistors T19, T20 is used to re-adjust sensor U↓ till Кн is energized.

The zeroing circuit inhibiting operation of fault memory when the integrated circuit power source becomes operationally ready is built around transistors T16, T18 and stabilizer diode Д26.

Right after closing the generator switch while a voltage of the 5-V source supplied to the base of transistor T16 is lower than stabilizing voltage of Д26, transistor T16 and, hence, transistor T18 are conductive. Logic "0" inhibiting operation of the memory circuit is taken off from collector T17. As the 5-V source becomes operationally ready, a voltage across the base of transistor T16 becomes higher than the voltage across the stabilizing voltage of Д26 which turns off transistors T16 and T18. Logic "1" appears across collector T18 to indicate canceling the zeroing signal.

After testing the БЗУНП355Г unit, the fault memory clearing is performed by supplying via the external resistor, terminal 64 +27 V to base T18.

Realized across elements У28, У27-4 and У21-3 is equation (8).

Re-multiplied with a subsequent negation across element У8 are inverse values of fault signals HU↑, HU↓, H∆U, $H_{К.З.}$. Storing the fault sum signal is accomplished (after operation of the amplifier, relay and level converter) by applying signal HΣ to У28/7. Then the fault sum signal obtained across output У28/12 is multiplied with signal $\overline{\text{Обн.}}$. Obtained after inversion across output У21/10 is signal HΣ transmitted by the unit via terminal 61.

The logic of unwanted oscillation signal (Вг is built around integrated circuits У12, У13 in compliance with equation (1). Logic "1" applies signal Вг to terminal 46 of the БСГБ1Б unit from interconnected outputs У13 via bias diodes У30 provided even one logic "0" is applied to the inputs of each of inverters У13. Logic "0" comes to inputs 13, 14 from У12/10 if logic "1" exists across inputs У12/8 ande12/9 which complies with the absence of signal HΣ across terminal 30 of the БСГБ1Б unit and absence of the INHIBITION 52 % signal in the БЗУНП355Г unit. Logic "0" is applied to input 8 of element У13 from output У12/12 provided logic "1" is applied to inputs 13, 14 of element У12 which testifies to the fact that the generator frequency is normal. After applying excitation to У13/7, logic "0" is backed up irrespective of state of inputs 13 and 14 of element У12. Logic "1" is fed to input У13/9 via terminal 47 whenever the БСГБ1Б unit is used in the БЗУНП355Г unit wherein disconnection versus f↓ is reversible.

Command Кн to energize the load contactor is shaped in compliance with equation (2). It is transmitted via terminal 41 of the БСГБ1Б unit from the outputs of integrated circuit У10.

Logic "1" appears across outputs У10 if the generator switch is in the GENERATOR ON (ГЕНЕРАТОР ВКЛЮЧЕН) position and excitation Вг is applied. That is, logic "0" is applied to inputs 13, 14 of element У10. Logic "0" shall exist across the said inputs if 27 V is supplied via the resistors to terminals 36 and 25 of the unit. A check for a reduced voltage is performed by applying signal U↓ to input У10/8 (output У8/10 is always equal to logic "1" owing to the absence of signal $U_{шг}$ in the given memory unit).

Disabling the absence of U↓ is accomplished by applying logic "0" to inputs 7 and 9 of integrated circuit У10 which appear upon canceling a zeroing signal and energizing the load contactor.

Inhibition of load contactor energizing is of no sense in case a voltage exists across the buses. This is true for the systems with the switching contactors for which the БЗУНП355Г unit is designed. That is why the voltage is not supplied to the inputs of sensor $U_{шг}$ (terminals 17 thru 20) and logic "0" is always present at input У8/8.

To adjust the БЗУНП355Г unit, signals from the sensors are brought out via the dividing inverters of elements У16 and У15 to terminals 48, 49, 51 thru 53, 55, 57.

3.12. Parallel operation unit БСГП1Е

To follow the description of operation of the БСГП1Е unit, consult the schematic diagram shown in Fig. 12.

The unit incorporates the functional groups mentioned under 3.1. It accomplishes the functions in compliance with equations (9, 10).

3.12.1. Operation of discriminator

A discriminator is a unit intended for ensuring voltage protection selectivity during parallel operation of the generators. As the voltage in the system of parallel operating generator goes down, disconnect an insufficially excited generator and apply inhibiting signal DU↓ to the protection versus U↓ of the generator whose reactive current is greater than an average rective current. As the voltage in the system goes up, the discriminator produces inhibiting signal DU↑ to the protection versus U↑ of the generator whose reactive current is less than an average reactive current making it possible for the protection versus U↑ to disconnect an overexcited generator.

Supplied via terminals 4 and 3 of the БСГП1Е unit to the discriminator input via diode switch Д3 thru Д6 is a voltage proportional to the difference of current of phase A of the given generator and an average current of phase A of parallel operating generators ΔJ_1 (Ref. Figs 13a, 14a).

The diode switch is commutated by line voltage $U_{вс}$ separated from the voltage of phase A and, hence, from the active component of current J_A by 90°.

Current flows to capacitors C5 and C6 from inputs 4, 3 during positive half-periods Uвс (Ref. dashed section of curve UΔJ in Figs 13b, 14b). So in case the reactive components of generator load current are equal (Ref. Fig. 13) an average value of voltage supplied to capacitors C5, C6 is equal to zero.

Another extremis, when the current difference exists owing to reactive components, is shown in Fig. 14.

In case the both current components are noto equal a value of the voltage across the capacitors is proportional to the difference of reactive components of the current of phase A of the given generator and an average current of phase A of parallel operating generators. A polarity of voltage across capacitors C5, C6 depends on the sign of deviation.

Parallel-connected to capacitors C5, C6 is a capacitive divider employing capacitors C7 and C8 whose center tap is connected to the 5-V source.

Voltage is supplied from the capacitors with respect to a level of +5 V to the inputs of two relays built around active elements У4, T2, T3 and У6, T7, T8, accordingly.

Depending on the polarity of voltage across the capacitors (at a definite value) this or that relay is energized. Exist across the relay output, for instance, across the collector of transistor T3 shall be logic "1" provided a potential below the level supplied to input У4/10 is supplied from the divider employing resistors R10, R11 to input 9 of operational amplifier У4. If the reactive currents of parallel operating generators differ but slightly, a voltage across capacitors C5, C6 is insufficient for tripping of the relays. The signals of logic "0" are picked off from the output of both relays (from the collectors of transistors T3 and T7) and fed to the logic via terminals 8 and 9.

3.12.2. Shaping signals Кпр and ПОС

Signal Кпр (ПОС) shaped in compliance with equation (9) is taken off by logic "1" from the collector of transistor in integrated circuit У7 (terminal 4). It is applied to the input of a three-stage amplifier connected into a common-emitter circuit employing the transistors of matrix У19. The transistors of matrix У19 complete the circuit of coil of a relay whose contacts apply ПОС to unshunt the protection. Besides, signal Кпр is brought out of the БСГП1Е unit via terminal 22 to be multiplied with the similar signal from a coupled БЗУНП355Г unit and amplified in the БУС9Б unit, and to energize contactor Кпр as well. To obtain signal Кпр, logic "0" shall exist across output У15/12. Logic "0" is obtained through feeling logic "1" to inputs У15-1.

Fed to input У15/13 is an inverse value of Нпр multiplied with Кн and to input У15/14, signal

$$(B_{пр} + B_{пр\ test}) + \bar{z} \cdot \overline{(U\downarrow + \Delta U)} \qquad (9).$$

So, signal Кпр across terminal 22 of the БСГП1Е unit shall have a value of

$$Кпр = (B_{пр} + B_{пр\ test}) \cdot [((B_{пр} + B_{пр\ test}) \cdot Кн \cdot \overline{Нпр} + Кн \cdot \overline{Нпр} + \bar{z} \cdot \overline{(U\downarrow + \Delta U)}] \qquad (10).$$

However, it no sense to take into account the second addend of this expression since the Нпр already includes signal $\bar{z} \cdot \overline{(U \downarrow + \Delta U)}$. After energizing contactor Кпр, signal квКпр transmitted by the unit from terminal 23 comes to terminal 21 of the БСГП1Е unit to be converted into a level of +5 V. Then the signal is used in the БСГБ1Б unit.

De-energizing of contactor Кпр is effected from the Впр switch or by canceling the command from contactor Кн.

4.12.3. Emergency de-energizing of contactor Кпр

Emergency de-energizing of contactor Кпр is accomplished by protection Нпр at a time delay of 2 s (equation (10)) versus total current imbalance ΔJ of parallel operating generators or in response to signal U↓ or ΔU.

After the unshunting relay trips and opens its contacts in response to signal Кпр, signal ΔJ proportional to the difference between the current of given generator and average current of parallel operating generators comes to inputs 1, 2 of the БСГП1Е unit from the equalizing circuit resistor. The imbalance current meter consists of rectifier У3; a filter comprising resistors R19, R20, R25 and capacitor C4; a differential couple employing transistors T5, T9; a stage employing transistor T10 having a positive feedback with transistor T9.

If the current imbalance is absent transistors T9 and T10 are conductive owing to an unbalance introduced with the help of resistor R39.

If ΔJ exceeding a tolerance value exists a voltage drop caused by an input signal across resistor R25 renders transistor T5 conductive. In this case, transistors T9, T10 get turned off stepwise. Logic "1" appears at the output of sensor (collector of transistor T10) to indicate that current imbalance exists. Signal ΔJ taken off from collector T10 is inverted and added with signal Кн $\bar{z} \cdot \overline{(U \downarrow + \Delta U)}$ across У11-2, the inverse value of the signal is fed to У11/6, and with signal Нпр, the inverse value of the signal is fed to У9/14. A sum obtained across У9/10 is multiplied by signal (Впр + B_{test}) across У14/1. A signal obtained across output У14/6 triggers a time delay circuit built around transistor T13 and transistor assembly У18. The time delay circuit is similar to a circuit described under 2.11. Signal $H_{пр}$ taken off the output of time delay circuit У18/6 goes to the logic of signal Кпр. Clearing of the memory of signal Нпр is accomplished by canceling signal Впр + B_{test}. Signal Кн $\bar{z} \cdot \overline{(U \downarrow + \Delta U)}$ used in the logic of signal Нпр is shaped in integrated circuits У13, У11-1 and goes via the external jumper between terminals 37 and 34 of the unit to input У11/6.

UNIT – MAINTENANCE PRACTICES

Operation of the unit may be both an on-condition maintenance and operation till an assigned service life expires.

The unit assigned service life is specified in the Certificate.

The unit operational status is checked by the built-in test system.

The on-condition maintenance allows using the unit till failure. Meant under failure is the unit status, which does not imply an accident causing an emergency landing of the helicopter or abortion of a mission.

Before takeoff, a faulty unit shall be replaced with a sound one available in the SPTA set.

The on-condition maintenance of the unit or maintenance till the assigned service life is expired shall be performed in a scope and at intervals specified in the Maintenance Schedule.

At the Manufacturer's the unit is subjected to adjustment and does not call for an additional adjustment in use. In case the unit fails, replace it with a new one and send a faulty unit to the Manufacturer for repair.

Prior to installing the unit on the helicopter, inspect it visually (Ref. a respective TC).

UNIT – STORAGE INSTRUCTIONS

1. The units packed and preserved by the Manufacturer shall be stored in permanent unheated rooms at an ambient temperature from +30 to –40 °C and relative humidity of up to 95 %.

   Vapors and gases that may provoke corrosion cannot be tolerated in the storerooms.

   The units placed in packing shall be kept on wooden racks.

   Regularly (once in six months) check the color of silica gel indicator.

   In case the silica gel indicator turns absolutely pink in color along the whole length of the cartridge, subject the units to depreservation and a repeated preservation.

2. To accomplish a repeated preservation of the unit:
   - examine the unit and, if necessary, wipe dirty areas with rags moistened with gasoline, grade Б-70 1012-72;
   - wrap the unit with subparchment 1760-68 and paraffined paper, grade БП-3-35 9569-79;
   - spread fabric bags with commercial silica gel 3956-76 1 kg per 1 m^2 of the bag surface and a cartridge with silica gel indicator 8984-75;
   - put the unit in a bag made of polyethylene film Mc, 150 to 200 μ thick, 10354-73, evacuate air from the bag until the film slightly sticks to the unit and solder up the last seam of the bag.

UNIT – SHIPMENT

The units packed and preserved by the Manufacturer may be transported by any type of transport to any distance and at any speed.

In case the preservation term is two years long, shipment shall be performed by a closed transport which ensures protection of the units against precipitation.